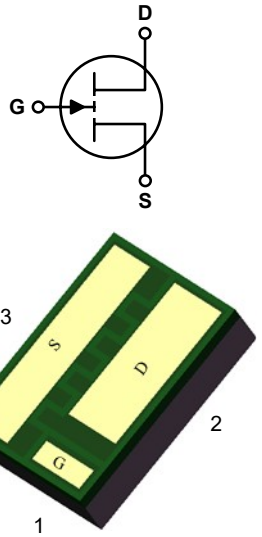
INN150LA070A

1. General description

GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in Flip chip LGA (FCLGA) with 3.2 mm x 2.2 mm package size.



2. Features

- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra-low on resistance
- Very small package size
- Zero reverse recovery charge

3. Applications

- Synchronous rectification
- Class-D audio
- High frequency DC-DC converter
- Communication base station
- Motor driver

4. Key performance parameters

Table 1 Key performance parameters at T_J = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	150	V
$R_{DS(on),max}$ @ V_{GS} = 5 V	7	mΩ
$Q_{G,typ}$ @ V_{DS} = 85V	7.6	nC
$I_{DS,Continuous}$	28	A
Q_{OSS}@ V_{DS} = 85V	47	nC

5. Pin information

Table 2 Pin information

PIN	Pin Description	Pin Function
1	Gate	Driver Gate
2	Drain	Power Drain
3	Source	Power Source

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN150LA070A	LGA 3.2x2.2	M01

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6. Maximum ratings

at T_J = 25 °C unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	150	V
I_D	Continuous current	28	A
	Pulsed (25˚C, T_{Pulse} = 300 μs)	120	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	˚C

7. Thermal characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	26	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	4.4	˚C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [1]	57	˚C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

8. Electric characteristics

at T_J = 25 °C, unless specified otherwise

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Voltage	150	-	-	V	V_{GS} = 0 V, I_D = 900 μA
I_{DSS}	Drain Source Leakage	-	8	45	μA	V_{GS} = 0 V, V_{DS} =120 V
I_{GSS}	Gate-to-Source Forward Leakage	-	1	32	μA	V_{GS} = 5 V
	Gate-to-Source Reverse Leakage	-	8	45	μA	V_{GS} = -4 V
$V_{GS(TH)}$	Gate Threshold Voltage	0.8	1.1	2.1	V	V_{DS} = V_{GS}, I_D = 5 mA
$R_{DS(on)}$	Drain-Source On-state Resistance	-	5.6	7	mΩ	V_{GS} = 5 V, I_D = 10 A
V_{SD}	Source-Drain Forward Voltage	-	1.2	-	V	I_S = 0.5 A, V_{GS} = 0 V

Table 7 Dynamic characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{iss}	Input Capacitance	-	865	-	pF	V_{GS} = 0 V, V_{DS} = 85 V
C_{oss}	Output Capacitance	-	280	-		V_{GS} = 0 V, V_{DS} = 85 V
C_{rss}	Reverse Transfer Capacitance	-	2.5	-		V_{GS} = 0 V, V_{DS} = 85 V
$C_{oss(er)}$	Energy Related C_{oss}	-	380	-		V_{GS} = 0 V, V_{DS} = 0 V to 85 V
$C_{oss(tr)}$	Time Related C_{oss}	-	555	-		V_{GS} = 0 V, V_{DS} = 0 V to 85 V
R_G	Gate resistance	-	2.3	-	Ω	f = 5MHz, drain open
Q_G	Total Gate Charge	-	7.6	-	nC	V_{GS} = 5 V, V_{DS} = 85 V, I_D=10 A
Q_{GS}	Gate to Source Charge	-	1.7	-		V_{DS} = 0 V to 85 V, I_D = 10 A
Q_{GD}	Gate to Drain Charge	-	1.3	-		V_{DS} = 0 V to 85 V, I_D = 10 A
$Q_{G(TH)}$	Gate Charge at Threshold	-	1.3	-		V_{DS} = 0 V to 85 V, I_D = 10 A
Q_{OSS}	Output Charge	-	47	-		V_{GS} = 0 V, V_{DS} = 0 V to 85 V

9. Electric characteristics diagrams

at T_J = 25 °C, unless specified otherwise

Fig. 1 Typical Output Characteristics (T_J=25°C)

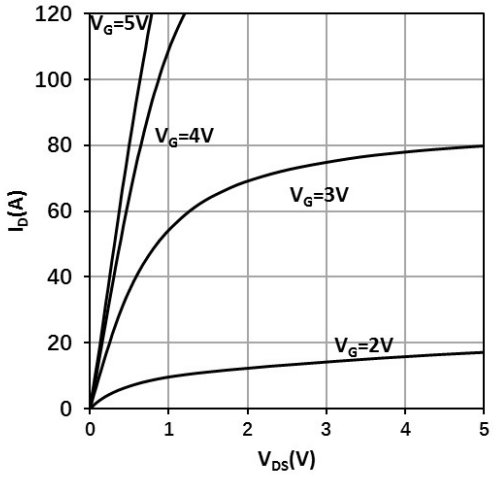


Fig. 2 Typical Output Characteristics (T_J=125°C)

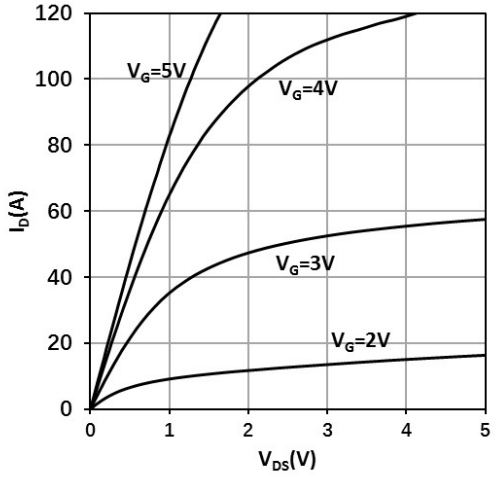


Fig. 3 Typical On-state Resistance (T_J=25°C)

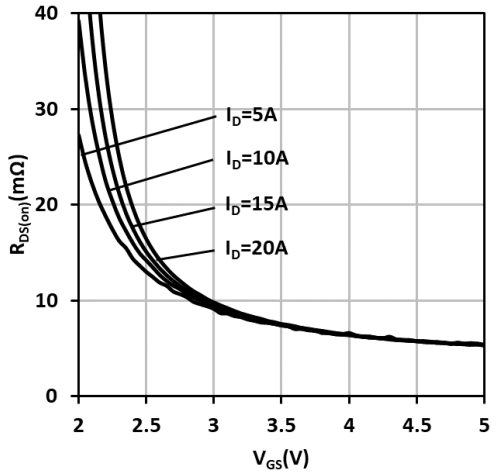


Fig. 4 Typical On-state Resistance (T_J=125°C)

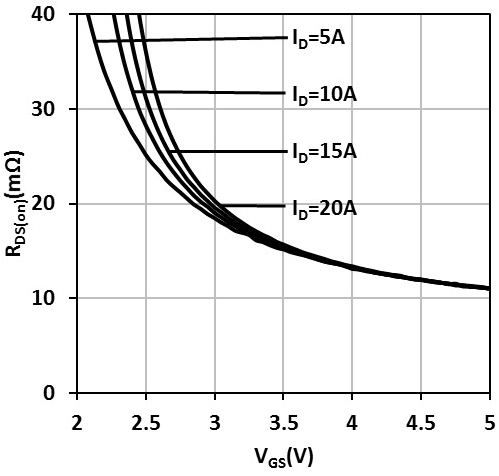


Fig. 5 Normalized On-State Resistance vs. Temp.

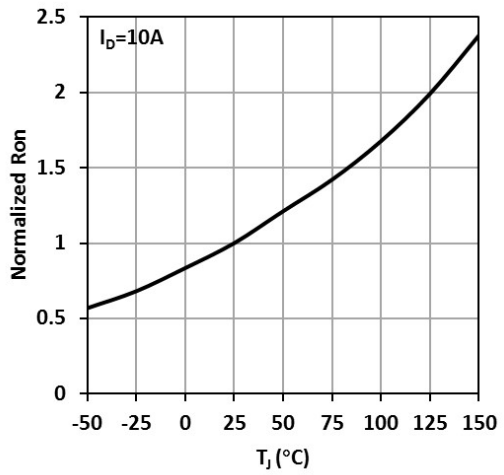


Fig. 6 Typical Transfer Characteristics

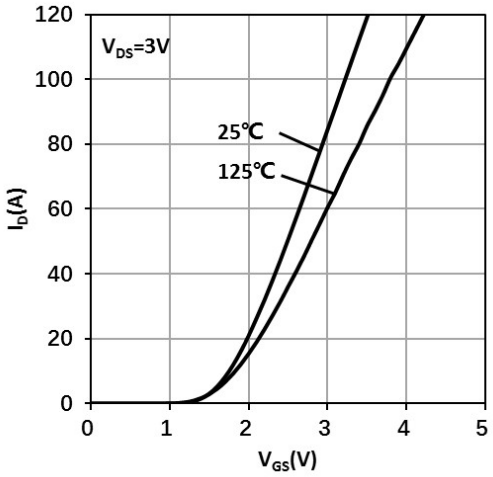


Fig. 7 Typ. Reverse Characteristics ($V_{GS}\leqslant 0, T_J$=25°C)

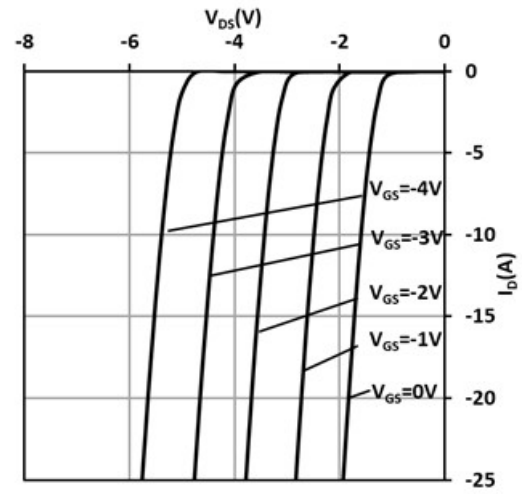


Fig. 8 Typ. Reverse Characteristics ($V_{GS}\geqslant 0, T_J$=25°C)

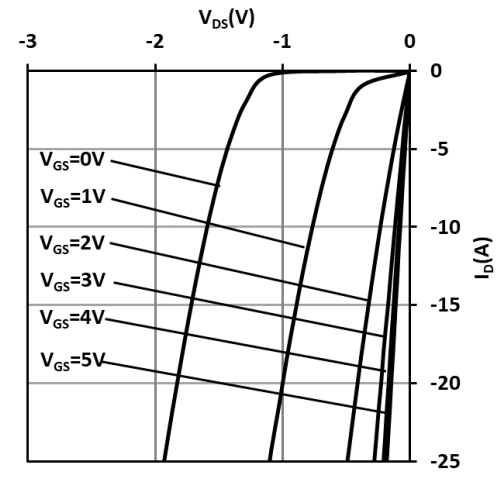


Fig. 9 Typ. Reverse Characteristics ($V_{GS}\leqslant 0, T_J=125°C$)

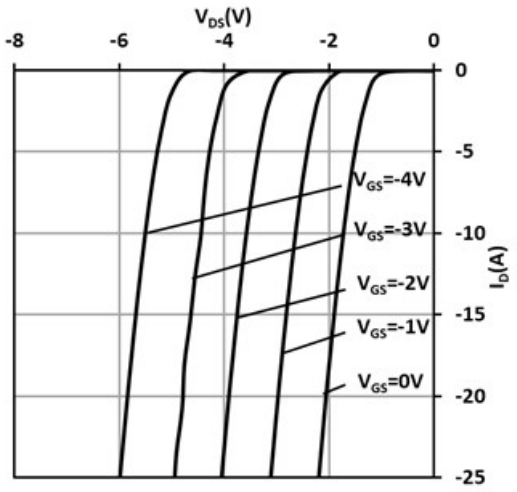


Fig. 10 Typ. Reverse Characteristics ($V_{GS}\geqslant 0, T_J=125°C$)

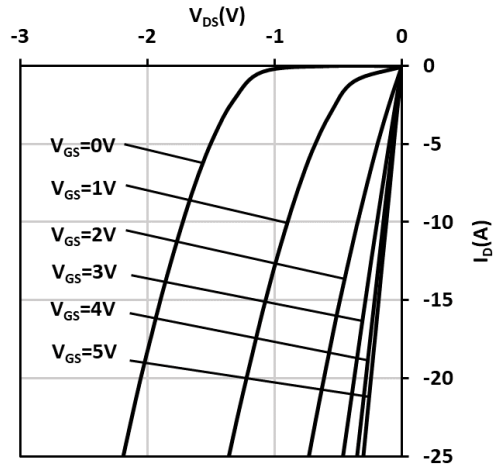


Fig. 11 Typ. Capacitances Characteristics

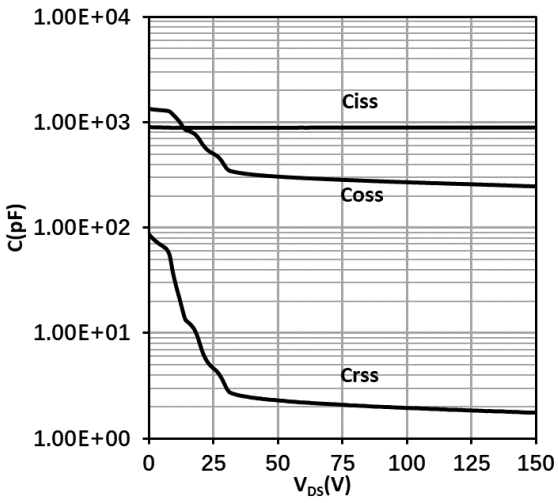


Fig. 12 Typ. Gate Charge

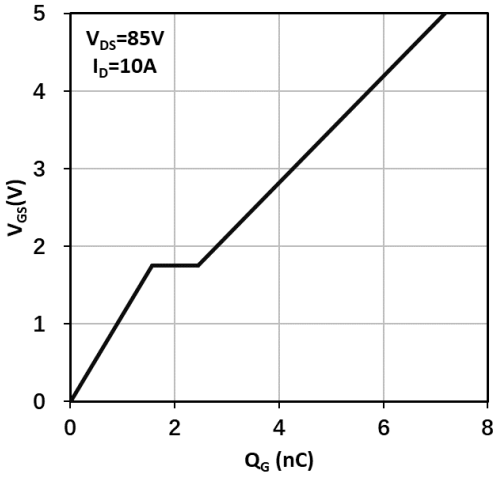


Fig. 13 Normalized Threshold Voltage vs. Temp.

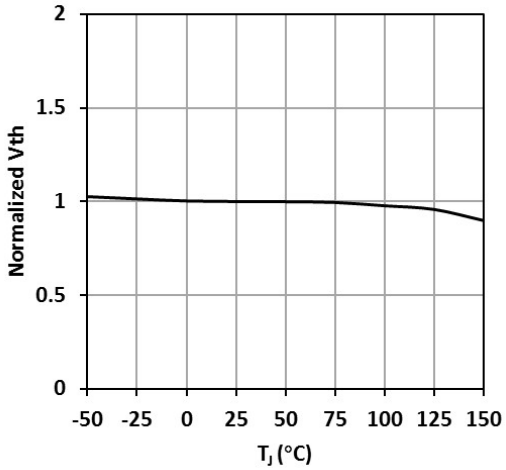


Fig. 14 Output Charge

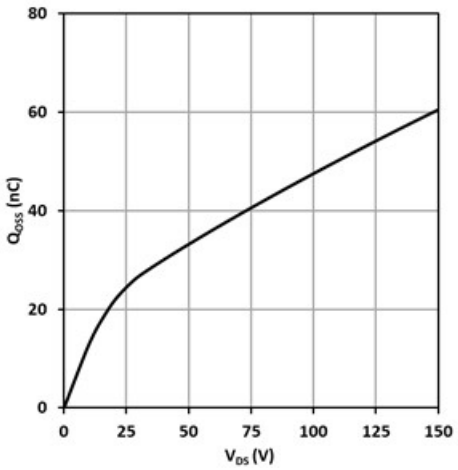


Fig. 15 Output Capacitance Stored Energy

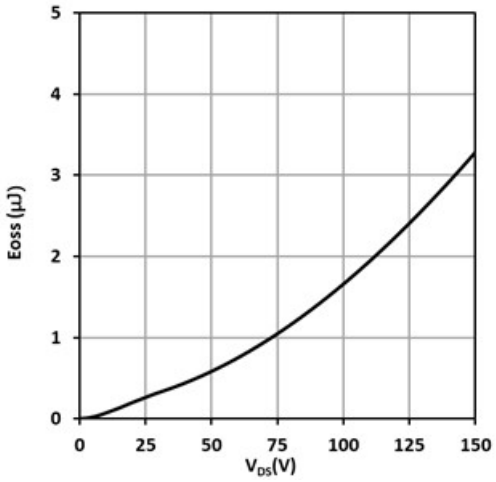


Fig. 16 Power Dissipation

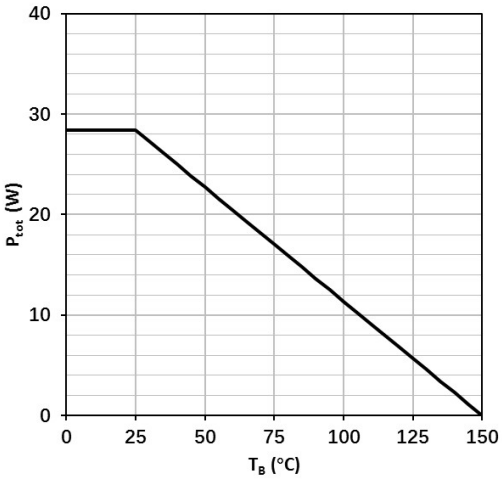
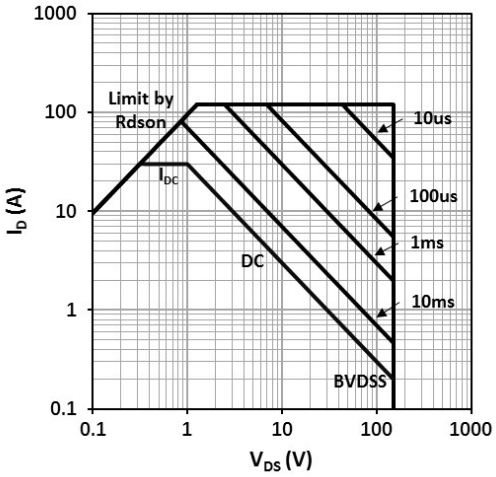
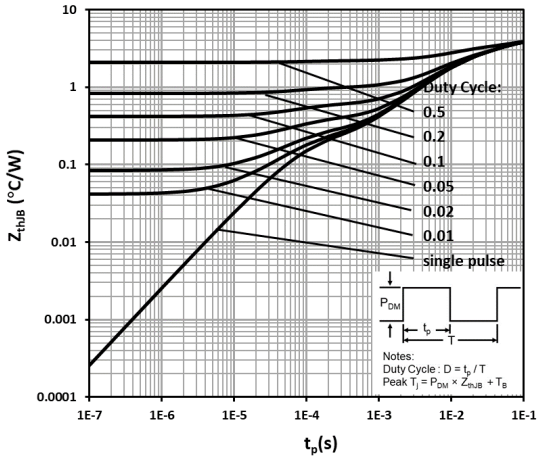


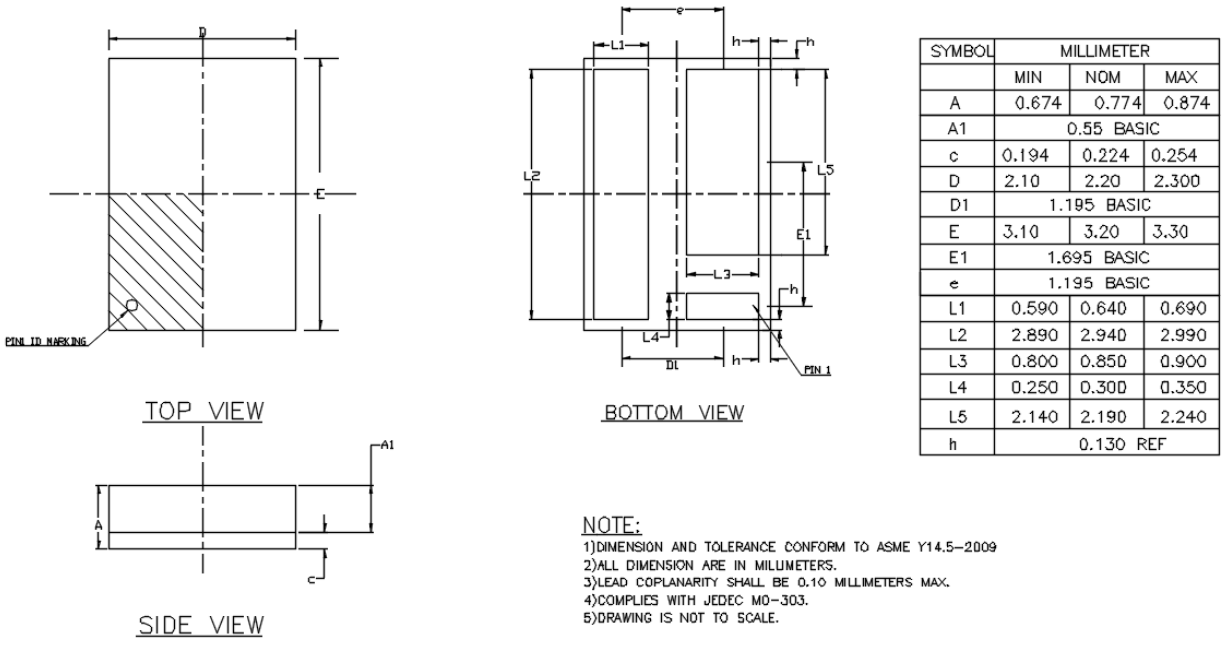
Fig. 17 Safe Operating Area	Fig. 18 Max. Transient Thermal Impedance





10. Package outlines

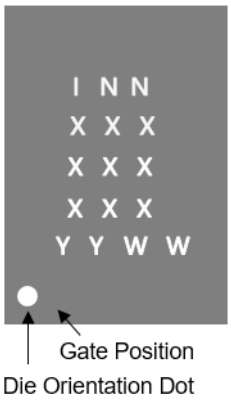
Package Reference



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.674	0.774	0.874
A1	0.55 BASIC		
c	0.194	0.224	0.254
D	2.10	2.20	2.300
D1	1.195 BASIC		
E	3.10	3.20	3.30
E1	1.695 BASIC		
e	1.195 BASIC		
L1	0.590	0.640	0.690
L2	2.890	2.940	2.990
L3	0.800	0.850	0.900
L4	0.250	0.300	0.350
L5	2.140	2.190	2.240
h	0.130 REF		

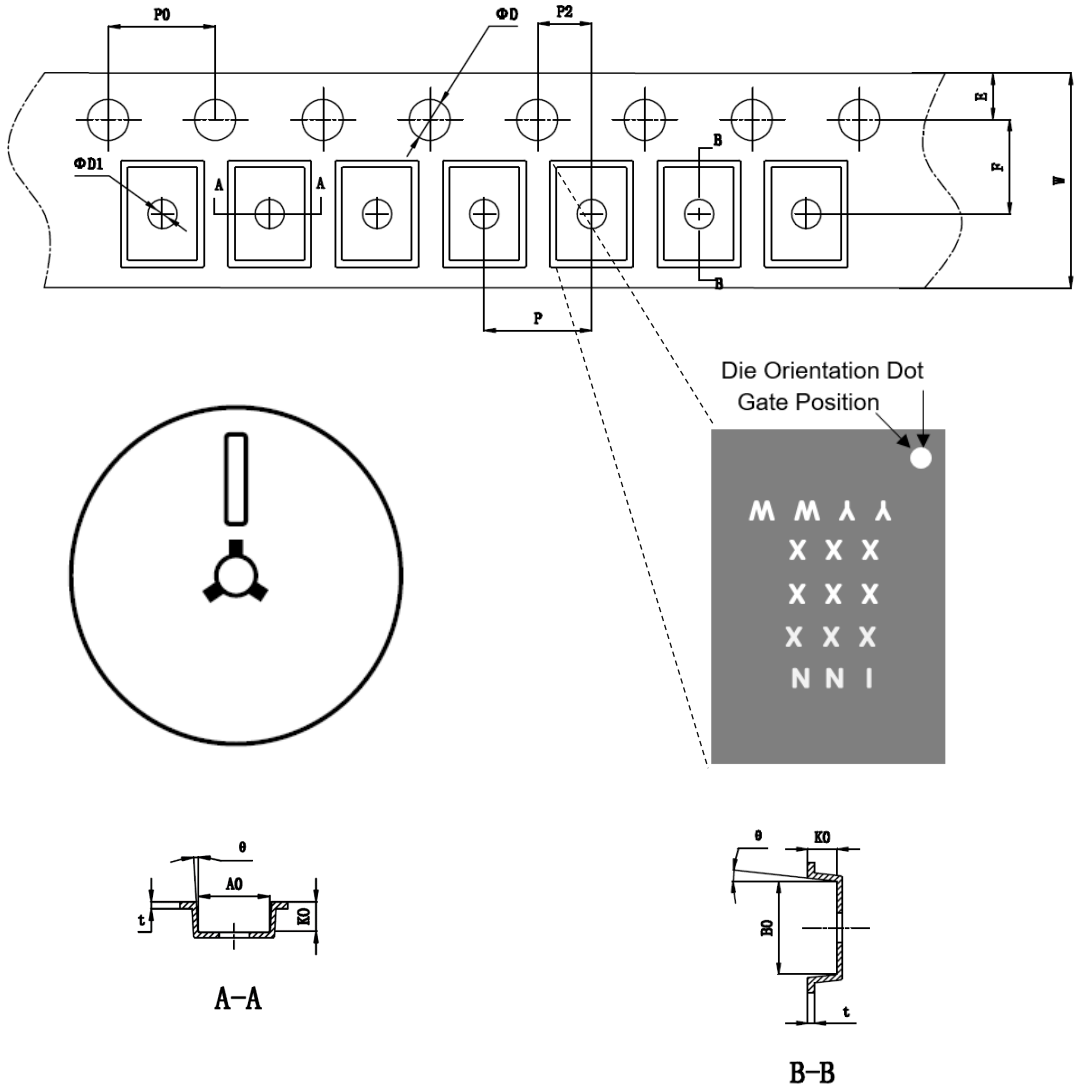
NOTE:
1)DIMENSION AND TOLERANCE CONFORM TO ASME Y14.5-2009
2)ALL DIMENSION ARE IN MILLIMETERS.
3)LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4)COMPLIES WITH JEDEC MO-303.
5)DRAWING IS NOT TO SCALE.

Marking Reference:



Marking Line 1 (INN)	Innoscience
Marking Line 2 (XXX)	Product code
Marking Line 3 (XXX)	Lot Code
Marking Line 4 (XXX)	
Marking Line 5 (YYWW)	Date code

11. Reel information



Symbol	Dimension(mm)			Symbol	Dimension(mm)		
	MIN	NOM	MAX		MIN	NOM	MAX
E	1.65	1.75	1.85	W	7.9	8.0	8.1
F	3.45	3.5	3.55	P	3.9	4.0	4.1
P2	1.95	2.0	2.05	A0	2.5	2.6	2.7
D	1.45	1.55	1.65	B0	3.4	3.5	3.6
D1	1.0	1.1	1.2	K0	1.0	1.1	1.2
P0	3.9	4.0	4.1	t	0.2	0.25	0.3
10P0	39.8	40	40.2	θ	5° TYP		

12. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2022-05-05	Rev 1.0 version release
1.1	2023-11-29	Rev 1.1 update Pin information& Electric characteristics & diagrams

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